REMARKS

Applicant thanks the Examiner for recognizing that claims 6, 8, 9, 16, 18, 38, 40, 41, 45, 46, 49, 50, 54, 55, 58, 59, 62 and 64 include allowable subject matter.

Claims 4, 5, 7, 10-15, 17, 20-26, 32-37, 39, 42-44, 48, 52-53, 57, 61, 63 and 65-75 were rejected as anticipated by U.S. Patent No. 5,221,428 (Ohsawa et al.).

As disclosed in the specification, prior to half-etching a board to form a lead-frame, the second planar surface includes semiconductor element mount regions 54 and a conductive coating film 56 that serves as a mask to define patterns for first pads (*e.g.*, FIG. 1A). After half-etching the board using the conductive pattern as a mask (FIG. 1B), first pads 55 are defined by the conductive patterns 56, and the die pads 59 are defined by the semiconductor element mount regions 54.

The independent claims have been amended to clarify that the sheet-like board member includes at least one unit, each of which includes a plurality of patterns or protuberances corresponding to first pads and also including a plurality of die pads corresponding to semiconductor element mount regions in the unit. An example of a "unit" is identified as 83 in FIG. 5A.

Including a plurality of patterns, or protuberances, and a plurality of die pads in each unit makes it possible to provide multiple circuit elements within a particular unit. That allows more complex circuitry to be included.

The Ohsawa et al. patent discloses a lead frame formed using a three-layered structure (thick metal 3, etch stop layer 2, thin metal 4). The main material of the lead frame is formed by etching the thick metal layer. The connections to an IC are formed by etching the thin metal layer.

In contrast to the claimed subject matter, each unit in the Ohsawa et al. patent is arranged for a single semiconductor element. There is no disclosure of a plurality of die pads

corresponding to a plurality of semiconductor element mount regions in a single unit. At least for that reason, the claims are not anticipated by the Ohsawa et al. patent.

Nor would that feature, or the subject matter of any of the independent claims, have been obvious from the Ohsawa et al. patent. Indeed, by emphasizing the trend toward a higher degree of integration (col. 1, lines 12-15), the Ohsawa et al. patent teaches away from an arrangement in which each unit would include a plurality of die pads corresponding to a plurality of semiconductor element mount regions. Instead, the Ohsawa et al. patent focuses on the need to provide a greater number of pins at a smaller pitch to access a single integrated circuit (IC). *See, e.g.*, col. 1, lines 16-20; col. 2, lines 26-30.

In view of the foregoing amendments and remarks, applicant respectfully requests reconsideration and allowance of all claims.

Enclosed is a check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 11/23/05

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